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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,052	03/30/2001	Sanjay Ramakrishna Pillay	1138-EP	8450

7590 06/03/2004

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EXAMINER	
CHU, GABRIEL L	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,052	PILLAY ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *1-6,16 and 17* is/are rejected.

7)☒ Claim(s) *7 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-6, 16, and 17 are rejected under 35 U.S.C. 102(a) as being anticipated by US 6131174 to Fischer et al. Referring to claim 1, Fischer et al. disclose a debug subsystem for testing a system-on-a-chip including an embedded processor and memory (From the abstract, "An interlocutor system and method is described that allows for at-speed testing of an embedded microcontroller at the control of an embedded digital signal processor in a system-on-a-chip architecture. The interlocutor system includes a buffer for temporarily storing test program data words output by the DSP and retrieved by the microcontroller being tested and a control circuit for controlling the microcontroller and DSP. The microcontroller, DSP, and interlocutor system are all located on a single integrated circuit.") comprising: at least one sub-block operable to: monitor a bus between the processor and the memory to detect program selected triggering events, count the number of triggering events detected (From line 10 of column 2, "A test program is downloaded into the on-chip memory along with a DSP support program. " Wherein the test program selects data words as triggering events. Further, from line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and when the number of triggering events reaches a program selected

threshold, generating a debugging signal (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer." Wherein the test program selects zero as the threshold. Further, from line 10 of column 2, "A test program is downloaded into the on-chip memory along with a DSP support program. ").

Referring to claim 2, Fischer et al. disclose the triggering events comprise memory accesses (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty.").

Referring to claim 3, Fischer et al. disclose the memory accesses are selected from the group including reads and writes (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty.").

Referring to claim 4, Fischer et al. disclose the triggering events comprise memory accesses within a selected address range (From line 28 of column 4, "The counter 44 is an up/down counter corresponding to the depth of the data latch 42 and having an EMPTY flag which is set when the counter 44 is at zero and a FULL flag which is set when the counter is at a maximum value corresponding to a full data latch

42. If the data latch 42 has a one data word capacity, the counter 44 may be a toggle flip-flop which assumes two states-one state, the EMPTY state, when the data latch is empty and capable of receiving a data word from the DSP 14, and another state, the FULL state, when the data latch 42 contains a data word ready to be retrieved by the microprocessor 12. If the data latch 42 has a multi-data word capacity, the counter 44 has a number of bits required for counting the number of data words which may be stored in the data latch 42." Wherein memory accesses occur within the range dictated by latch capacity.).

Referring to claim 5, Fischer et al. disclose the debugging signal is operable to freeze a clock timing the operation of the processor (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer.").

Referring to claim 6, Fischer et al. disclose the debugging signal comprises an interrupt to the processor (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer." Wherein preventing the microcontroller from attempting to retrieve data interrupts the processor.).

Referring to claim 16, Fischer et al. disclose a method of debugging a single-chip system including an embedded processor and memory (From the abstract, "An interlocutor system and method is described that allows for at-speed testing of an embedded microcontroller at the control of an embedded digital signal processor in a system-on-a-chip architecture. The interlocutor system includes a buffer for temporarily

storing test program data words output by the DSP and retrieved by the microcontroller being tested and a control circuit for controlling the microcontroller and DSP. The microcontroller, DSP, and interlocutor system are all located on a single integrated circuit.") comprising the steps of: selecting programmable triggering event parameters, monitoring transactions between the processor and the memory to detect triggering events corresponding to the selected triggering event parameters, counting the number of triggering events detected (From line 10 of column 2, "A test program is downloaded into the on-chip memory along with a DSP support program. " Wherein the test program selects data words as triggering events. Further, from line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and when the number of triggering events reaches a programmed predetermined threshold, generating a debugging signal (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer." Wherein the test program selects zero as the threshold. Further, from line 10 of column 2, "A test program is downloaded into the on-chip memory along with a DSP support program. ").

Referring to claim 17, Fischer et al. disclose said step of selecting triggering event parameters comprises the substeps of: selecting a triggering memory access type (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a

counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and selecting a triggering address range (From line 28 of column 4, "The counter 44 is an up/down counter corresponding to the depth of the data latch 42 and having an EMPTY flag which is set when the counter 44 is at zero and a FULL flag which is set when the counter is at a maximum value corresponding to a full data latch 42. If the data latch 42 has a one data word capacity, the counter 44 may be a toggle flip-flop which assumes two states-one state, the EMPTY state, when the data latch is empty and capable of receiving a data word from the DSP 14, and another state, the FULL state, when the data latch 42 contains a data word ready to be retrieved by the microprocessor 12. If the data latch 42 has a multi-data word capacity, the counter 44 has a number of bits required for counting the number of data words which may be stored in the data latch 42." Wherein memory accesses occur within the range dictated by latch capacity.).

Allowable Subject Matter

3. Claims 7 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 8-15 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments filed 29 March 2004 have been fully considered but they are not persuasive. Referring to Applicant's argument that Fischer et al. do not teach a program selectable trigger event type or a program selectable trigger event count threshold, Examiner has further rejected the claims as written. Firstly, Applicant has not, in claims 1 or 16, claimed an "event type". Secondly, Fischer et al. disclose that the event selected for monitoring is a data word, whose threshold was chosen to be zero, from line 28 of column 4, "The counter 44 is an up/down counter corresponding to the depth of the data latch 42 and having an EMPTY flag which is set when the counter 44 is at zero and a FULL flag which is set when the counter is at a maximum value corresponding to a full data latch 42."

Applicant further argues that the circuit disclosed by Fischer et al. is fixed rather than programmable, but this is not the case. Fischer et al. teach downloading the test program onto the chip memory, from line 22 of column 3 (with emphasis), "A test program to be run on the microcontroller and a support program to be executed by the DSP 14 during a test is downloaded to the **RAM** 40 from the external memory 8 through the I/O control circuit 36 and DSP 14.", clearly showing alterability.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

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